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U.S. PATENT DOCUMENTS

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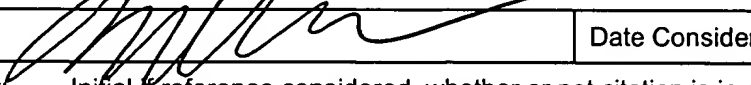
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FOREIGN PATENT DOCUMENTS

Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Nakamura, Kazuyuki et al., SP 24.6: A 500MHz 4Mb CMOS Pipeline-Burst Cache SRAM with Point-to-Point Noise Reduction Coding I/O, 1997 IEEE International Solid State Circuits Conference, Digest of Technical Papers, First Edition, February 1997, pp. 406-407.

Examiner		Date Considered	12/5/03
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